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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,009	08/28/2006	Yoshinobu Kono	082416-001400US	4829

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EXAMINER	
CAO, PHAT X	
ART UNIT	**PAPER NUMBER**
2814	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,009	KONO, YOSHINOBU	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Terashima (US 5,372,954).

Regarding claims 1 and 9, Terashima (Fig. 6) discloses an insulated gate semiconductor device, comprising: a first semiconductor region (2B) having a first conductivity type (column 8, lines 6-15); second semiconductor regions (1) having a second conductivity type (column 8, lines 6-15), formed in one principal surface of the first semiconductor region (2B); third semiconductor regions (3) having the second conductivity type (column 7, lines 39-47), formed in surface regions of the other principal surface of said first semiconductor region (2B); fourth semiconductor regions (4) having the first conductivity type (column 7, lines 39-47), formed in surface regions of the third semiconductor regions (3); a first electrode (8) electrically connected to the fourth semiconductor regions (4); a control electrode (6) disposed, via an insulating film (5), on the other principal surface between said first semiconductor region (2B) and the fourth semiconductor regions (4); and a second electrode (9) electrically connected to the second semiconductor regions (1), wherein the insulated gate semiconductor device comprises: a fifth semiconductor region (12) having the first conductivity type (column 8,

lines 6-15), formed in the one principal surface of the first semiconductor region (2B) so as to be adjacent to the second semiconductor regions (1); and a sixth semiconductor region (11) having the second conductivity type (column 8, lines 6-15), formed between the fifth semiconductor region (12) and the first semiconductor region (2B).

Regarding claims 2-3, Terashima (Fig. 6) further discloses that the sixth semiconductor region (11) is formed between a side of the fifth semiconductor region (12) closer to the other principal surface and the first semiconductor region (2B), and the fifth semiconductor region (12) is formed so as to be more prominent than the second semiconductor region (1).

Regarding claim 8, Terashima (Fig. 6) also discloses that the first semiconductor region comprises a first region (2B) and second regions (2A) higher in impurity concentration than the first region (2B) (column 8, lines 6-15), and the second regions (2A) are adjacent to the fifth semiconductor region (12).

3. Claims 1-2, 4, 6 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakurai (US 5,264,378).

Regarding claims 1 and 9, Sakurai (Fig. 6) discloses an insulated gate semiconductor device, comprising: a first semiconductor region (3) having a first conductivity type; second semiconductor regions (1) having a second conductivity type, formed in one principal surface of the first semiconductor region (3); third semiconductor regions (4) having the second conductivity type, formed in surface regions of the other principal surface of said first semiconductor region (3); fourth semiconductor regions (5) having the first conductivity type (column 9, lines 4-6), formed in surface regions of the

third semiconductor regions (4); a first electrode (E) electrically connected to the fourth semiconductor regions (4); a control electrode (6) disposed, via an insulating film (7), on the other principal surface between said first semiconductor region (3) and the fourth semiconductor regions (4); and a second electrode (10) electrically connected to the second semiconductor regions (1), wherein the insulated gate semiconductor device comprises: a fifth semiconductor region (15) having the first conductivity type, formed in the one principal surface of the first semiconductor region (3) so as to be adjacent to the second semiconductor regions (1); and a sixth semiconductor region (12) having the second conductivity type, formed between the fifth semiconductor region (15) and the first semiconductor region (3).

Regarding claims 2, 4, and 6, Sakurai (Fig. 6) further discloses that the sixth semiconductor region (12) is formed between a side of the fifth semiconductor region (15) closer to the other principal surface and the first semiconductor region (3), a width of the sixth semiconductor region (12) (corresponding to a width formed between element 15 and element 1) is smaller than a width of the fifth semiconductor region (15), and concentration of an impurity of the second conductive type in the sixth semiconductor region (12) is about 10^15 cm^-3 (column 6, lines 41-44).

4. Claims 1-2, 5, 7, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Majumdar et al (US 2002/0153586).

Regarding claims 1 and 9, Majumdar (Fig. 11) discloses an insulated gate semiconductor device, comprising: a first semiconductor region (201) having a first conductivity type; second semiconductor regions (240) having a second conductivity

type, formed in one principal surface of the first semiconductor region (201); third semiconductor regions (203) having the second conductivity type, formed in surface regions of the other principal surface of said first semiconductor region (201); fourth semiconductor regions (205) having the first conductivity type, formed in surface regions of the third semiconductor regions (203); a first electrode (209) electrically connected to the fourth semiconductor regions (205); a control electrode (206) disposed, via an insulating film (207), on the other principal surface between said first semiconductor region (201) and the fourth semiconductor regions (203); and a second electrode (212) electrically connected to the second semiconductor regions (240), wherein the insulated gate semiconductor device comprises: a fifth semiconductor region (241) having the first conductivity type, formed in the one principal surface of the first semiconductor region (201) so as to be adjacent to the second semiconductor regions (240); and a sixth semiconductor region (202) having the second conductivity type, formed between the fifth semiconductor region (241) and the first semiconductor region (201).

Regarding claims 2 and 7, Majumdar (Fig. 11) further discloses that the sixth semiconductor region (202) is formed between a side of the fifth semiconductor region (241) closer to the other principal surface and the first semiconductor region (201), and the fifth semiconductor region (241) is formed so as not to face the third semiconductor region (203).

Regarding claim 5, Majumdar (Fig. 11) further discloses that the sixth semiconductor (202) is formed such that at least a part of the fifth semiconductor region

(241) (see the rightmost region 241 formed in section 221) contacts the first semiconductor region (201).

Regarding claim 8, Majumdar (Fig. 11) also discloses that the first semiconductor region comprises a first region (201) and second regions (241) (the rightmost region 241) higher in impurity concentration than the first region (201), and the second regions (241) (see rightmost region 241 formed in section 221) are adjacent to the fifth semiconductor region (202).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/P. X. C./
Primary Examiner, Art Unit 2814

/Phat X Cao/
Primary Examiner, Art Unit 2814